

In the Claims

1 1. (Previously Presented) A switch comprising:

2 a plurality of field effect transistors connected in series, each field effect transistor
3 including a gate, a source, and a drain, each gate having a gate width and a gate length;

4 said gate length of one of said series connected field effect transistors being a different
5 size from said gate length of another series connected field effect transistor.

1 2. (Previously Presented) The switch as claimed in claim 1, wherein said gate of one of
2 said plurality of series connected field effect transistor has a longer gate length than said gate of
3 said other series connected field effect transistor.

1 3. (Original) The switch as claimed in claim 1, wherein said gate of one of said plurality
2 of series connected field effect transistor has a distance to its drain port that is less than a
3 distance to its source port.

1 4. (Original) The switch as claimed in claim 1, wherein said gate of one of said plurality
2 of series connected field effect transistor has a distance to its source port that is less than a
3 distance to its drain port.

1 5. (Original) The switch as claimed in claim 3, wherein said gate of said other series
2 connected field effect transistor has a distance to its source port that is equal to a distance to its
3 drain port.

1 6. (Original) The switch as claimed in claim 4, wherein said gate of said other series
2 connected field effect transistor has a distance to its source port that is equal to a distance to its
3 drain port.

1 7. (Original) The switch as claimed in claim 1, wherein the different gate sizes increase a
2 parasitic capacitance within the switch.

1 8. (Original) A switch comprising:

2 a plurality of dual-gate field effect transistors connected in series, each dual-gate field
3 effect transistor including two gates, a source, and a drain;

4 one of said series connected dual-gate field effect transistors having a modified gate
5 therein that is of a different size from gates of other series connected dual-gate field effect
6 transistors.

1 9. (Original) The switch as claimed in claim 8, wherein said modified gate of said series
2 connected dual-gate field effect transistor has a longer gate length and/or gate width than gates of
3 said other series connected dual-gate field effect transistor.

1 10. (Original) The switch as claimed in claim 8, wherein said modified gate of said series
2 connected dual-gate field effect transistor has a distance to its drain port that is less than a
3 distance to its source port.

1 11. (Original) The switch as claimed in claim 8, wherein said modified gate of said series
2 connected dual-gate field effect transistor has a distance to its source port that is less than a
3 distance to its drain port.

1 12. (Original) The switch as claimed in claim 10, wherein gates of said other series
2 connected dual-gate field effect transistors have a distance to its source port that is equal to a
3 distance to its drain port.

1 13. (Original) The switch as claimed in claim 11, wherein gates of said other series
2 connected dual-gate field effect transistors have a distance to its source port that is equal to a
3 distance to its drain port.

1 14. (Original) The switch as claimed in claim 8, wherein a second series connected dual-
2 gate field effect transistor has a modified gate therein that is of a different size from gates of
3 other series connected dual-gate field effect transistors.

1 15. (Original) The switch as claimed in claim 8, wherein said dual-gate field effect
2 transistors are high-electron-mobility-transistors.

1 16. (Original) The switch as claimed in claim 8, wherein the different gate sizes increase
2 a parasitic capacitance within the switch.

1 17. (Original) The switch as claimed in claim 8, wherein said dual-gate field effect
2 transistors include a transistor connection segment between said gates and a heavily doped cap
3 layer fabricated upon said transistor connection segment between said gates.

1 **Claim18 (Cancelled)**

1 19. (Previously Presented) A high-electron-mobility-transistor, comprising:
2 two gate fingers;
3 a transistor connection segment between said gate fingers; and
4 a heavily doped cap layer fabricated upon said transistor connection segment between
5 said gate fingers;
6 said gate fingers being of different sizes.

1 20. (Original) The high-electron-mobility-transistor as claimed in claim 19, wherein one
2 of said gate fingers has a distance to its source port that is less than a distance to its drain port.

1 21. (Original) The high-electron-mobility-transistor as claimed in claim 19, wherein one
2 of said gate fingers has a distance to its drain port that is less than a distance to its source port.

1 22. (Original) A radio frequency single pole double throw switch, comprising:
2 a receiver port;
3 a transmitter port;
4 an antenna port;
5 a receiver section connecting said receiver port to said antenna; and
6 a transmitter section connecting said transmitter port to said antenna;
7 said receiver section including a plurality of dual-gate field effect transistors connected in
8 series, each dual-gate field effect transistor including two gates, a source, and a drain such that
9 one of said series connected dual-gate field effect transistors has a modified gate therein that is of
10 a different size from gates of other series connected dual-gate field effect transistors.

1 23. (Original) The radio frequency single pole double throw switch as claimed in claim
2 22, wherein a source of said modified gate transistor is connected to said receiver port.

1 24. (Original) The radio frequency single pole double throw switch as claimed in claim
2 22, wherein a drain of said modified gate transistor is connected to said antenna port.

1 25. (Original) The radio frequency single pole double throw switch as claimed in claim
2 22, wherein a second series connected dual-gate field effect transistor has a second modified gate
3 therein that is of a different size from gates of other series connected dual-gate field effect
4 transistors.

1 26. (Original) The radio frequency single pole double throw switch as claimed in claim
2 25, wherein a source of said modified gate transistor is connected to said receiver port and a
3 drain of said second modified gate transistor is connected to said antenna port.

1 27. (Original) The radio frequency single pole double throw switch as claimed in claim
2 22, wherein said dual-gate field effect transistors are high-electron-mobility-transistors.

1 28. (Original) The radio frequency single pole double throw switch as claimed in claim
2 22, wherein said modified gate of said series connected dual-gate field effect transistor has a
3 longer gate length and/or gate width than gates of said other series connected dual-gate field
4 effect transistor.

1 29. (Original) The radio frequency single pole double throw switch as claimed in claim
2 22, wherein said modified gate of said series connected dual-gate field effect transistor has a
3 distance to its drain port that is less than a distance to its source port.

1 30. (Original) The radio frequency single pole double throw switch as claimed in claim
2 22, wherein said modified gate of said series connected dual-gate field effect transistor has a
3 distance to its source port that is less than a distance to its drain port.

1 31. (Original) The radio frequency single pole double throw switch as claimed in claim
2 29, wherein gates of said other series connected dual-gate field effect transistors have a distance
3 to its source port that is equal to a distance to its drain port.

1 32. (Original) The radio frequency single pole double throw switch as claimed in claim
2 30, wherein gates of said other series connected dual-gate field effect transistors have a distance
3 to its source port that is equal to a distance to its drain port.

1 33. (Original) The radio frequency single pole double throw switch as claimed in claim
2 22, wherein the different gate sizes increase a parasitic capacitance within the switch.

1 34. (Original) The radio frequency single pole double throw switch as claimed in claim
2 22, wherein said dual-gate field effect transistors include a transistor connection segment
3 between said gates and a heavily doped cap layer fabricated upon said transistor connection
4 segment between said gates.

1 35. (Previously Presented) A radio frequency single pole double throw switch,
2 comprising:

3 a receiver port;

4 a transmitter port;

5 an antenna port;

6 a receiver section connecting said receiver port to said antenna; and

7 a transmitter section connecting said transmitter port to said antenna;

8 said receiver section including,

9 a first receiver dual-gate high electron mobility transistor having
10 gates of different lengths, and

11 a second receiver dual-gate high electron mobility transistor having
12 gates of different lengths.

1 36. (Previously Presented) The radio frequency single pole double throw switch as
2 claimed in claim 35, wherein the source of said first receiver dual-gate high electron mobility
3 transistor is connected to said receiver port.

1 37. (Previously Presented) The radio frequency single pole double throw switch as
2 claimed in claim 35, wherein the drain of said second receiver dual-gate high electron mobility
3 transistor is connected to said antenna port.

1 38. (Previously Presented) The radio frequency single pole double throw switch as
2 claimed in claim 35, wherein said transmitter section includes a first transmitter dual-gate high
3 electron mobility transistor having gates of different lengths and a second transmitter dual-gate
4 high electron mobility transistor having gates of different lengths.

1 39. (Previously Presented) The radio frequency single pole double throw switch as
2 claimed in claim 38, wherein the source of said first transmitter dual-gate high electron mobility
3 transistor is connected to said receiver port and the drain of said second transmitter dual-gate
4 high electron mobility transistor is connected to said antenna port.

1 40. (Previously Presented) The radio frequency single pole double throw switch as
2 claimed in claim 35, wherein a first gate of said first receiver dual-gate high electron mobility
3 transistor has a longer gate length and/or gate width than a second gate of said first receiver dual-
4 gate high electron mobility transistor.

1 41. (Previously Presented) The radio frequency single pole double throw switch as
2 claimed in claim 35, wherein a first gate of said first receiver dual-gate high electron mobility
3 transistor has a distance to its drain port that is less than a distance to its source port.

1 42. (Previously Presented) The radio frequency single pole double throw switch as
2 claimed in claim 35, wherein a first gate of said second receiver dual-gate high electron mobility
3 transistor has a distance to its source port that is less than a distance to its drain port.

1 **Cancelled Claims 43-44**

1 45. (Previously Presented) The radio frequency single pole double throw switch as
2 claimed in claim 35, wherein the different gate lengths increase a parasitic capacitance within the
3 switch.

1 46. (Previously Presented) The radio frequency single pole double throw switch claimed
2 in claim 35, wherein the different gate lengths improve the linearity without impacting the ESD
3 and EOS ruggedness.

1 47. (Currently Amended) A series connected dual-gate transistor, comprising:
2 a first gate; and
3 a second gate;
4 said first gate having a gate width and a gate length;
5 said second gate having a gate width and a gate length;
6 said gate length of said first gate being a different size from said gate length of said
7 second gate;
8 said gate width of said first gate being a different size from said gate width of said second
9 gate.

1 **Claims 48-50 (Cancelled)**